NEC

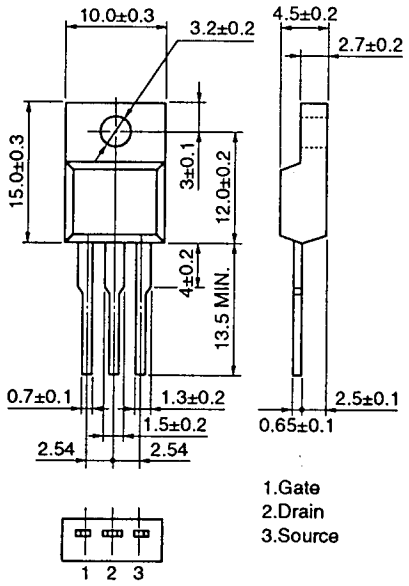
MOS Field Effect Power Transistors

2SK3059

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.



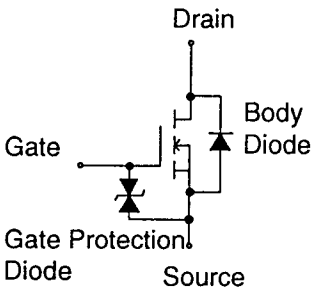
MP-45F (ISOLATED TO-220)

FEATURES

- Low On-State Resistance
  - $R_{DS(on)1}$ = 15mΩ Max. (VGS=10V,ID=25A)
  - $R_{DS(on)2}$ = 23mΩ Max. (VGS= 4V,ID=25A)
- Low C_{iss} C_{iss} = 2550pF Typ.
- Built-in Gate Protection Diode
- Isolated TO-220 Package

ABSOLUTE MAXIMUM RATINGS(Ta=25℃)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current(DC)	$I_{D(DC)}$	± 50	A
Drain Current(pulse)*	$I_{D(pulse)}$	±200	A
Total Power Dissipation(T_c=25℃)	P_T	30	W
Total Power Dissipation(T_a=25℃)	P_T	2.0	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature	T_{stg}	-55 to +150	℃



* PW≦10μs, Duty Cycle≦1%

THRMAL RESISTANCE

Channel to Case	Rth(ch-c)	4.17	℃/W
Channel to Ambient	Rth(ch-a)	62.5	℃/W

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this deveice acutally used, an addtional protection circiut is externally required if voltage exceeding the rated voltage may be applied to this device.

This information in this document is being issued in advance of the production cycle for the device. The parameter for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Document No.D13098EJ2V0PM00
Date Published Mar 1998

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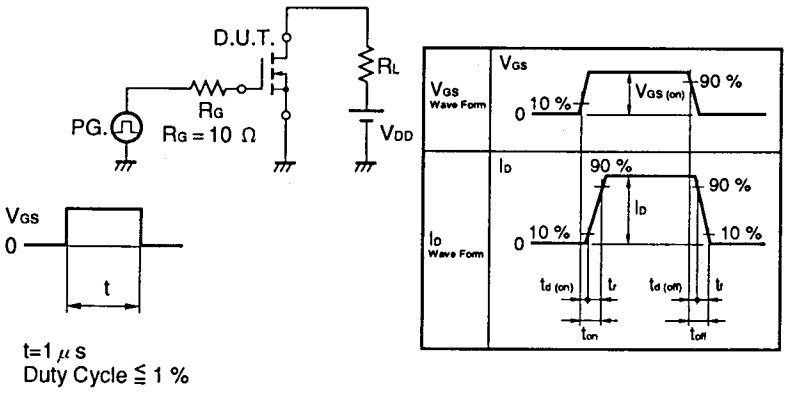
ELECTRICAL CHARACTERISTICS(Ta=25℃)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source	$R_{DS(on)1}$	V_{GS}=10V, I_D=25A		11	15	mΩ
On-state Resistance	$R_{DS(on)2}$	V_{GS}= 4V, I_D=25A		16	23	mΩ
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	1.0	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=10V, I_D=25A	15	30		S
Drain Leakage Current	I_{DSS}	V_{DS}=60V, V_{GS}=0			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0			±10	μA
Input Capacitance	C_{iss}	V_{DS}=10V		2550		pF
Output Capacitance	C_{oss}	V_{GS}=0		700		pF
Reverse Transfer Capacitance	C_{rss}	f=1MHz		250		pF
Turn-On Delay Time	$t_{d(on)}$	I_D=25A		30		ns
Rise Time	t_r	$V_{GS(on)}$=10V		400		ns
Turn-Off Delay Time	$t_{d(off)}$	V_{DD}=30V		170		ns
Fall Time	t_f	R_G=10Ω		200		ns
Total Gate Charge	Q_G	I_D=50A		50		nC
Gate to Source Charge	Q_{GS}	V_{DD}=48V		5.0		nC
Gate to Drain Charge	Q_{GD}	$V_{GS(on)}$=10V		15		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F=50A,V_{GS}=0		1.0		V
Reverse Recovery Time	t_{rr}	I_F=50A,V_{GS}=0		80		ns
Reverse Recovery Charge	Q_{rr}	di/dt=100A/μs		20		nC

Test Circuit 1 Switching Time



t=1 μs
Duty Cycle ≦ 1 %

Test Circuit 2 Gate Charge